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REVIEW OF I2C PROTOCOL

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ABSTRACT : I2C protocol provides easy communication without data loss. It also gives excellent speed compared to other protocols.I2C uses only two wire for communication.It. is light weight, economical and omnipresent. It also increases data transfer rate. The objective to develop the protocol is to get high speed communication and to control registers inside the devices as well as the data that can be saved on registers, through this we are able to control various parameters. I2C is used in data surveillance for accuracy and efficiency. The design method is developed in VHDL, simulated on MODELSIM or Xilinx and can be implemented on FPGA board
Keywords: *I2C protocol, Data surveillance, VHDL, ModelSim, SDA, SCL*

1. Literature Survey

There are many reasons for using serial interface design many more important application includes serial communication like sensors communication with personal computer. Many common Embedded system peripherals, such as anolog-to-digital and digital-to-anlaog convetors, LCDs, and temperature sensors, support serial interfaces.

Serial interface allow processors to communicate without the need for shared memory and the problems they can create. There are Serial communication protocols like UART,CAN,USB,SPI, Inter IC. USB,SPI and UARTS are all just one type to point type protocol. USB uses multiplexer to communicate with other devices. Only I^2C and CAN protocol uses software addressing. But only I^2C is very simple to design and easy to maintain.

	UART	**CAN**	**USB**	**SPI**	**I^2C**
PRONS	Well known Simple	Secure fast	Secure,fast,plug and play	Fast,low,cost,universally accepted,large portfolio	Simple,plug and play,cost effective,universally acceptd
CONS	Limited functionality, Point to point	Complex, liumited portfolio, Automotive oriented	Powerful master required, No plug and play software, Extra drivers required	No plug and play hardware, No fixed standard	Limited no. Of components due to capacitance effect

TableI:Comparisions of different protocols

2. INTRODUCTION

The physical size and power requirement of IC get reduce over the years. The main reason for that is more number of transistors can be integrated into smaller size and less number of interconnections wire present in between ICs can possible. The actual circuitry of the IC is much smaller than the packaging of the IC but it requires larger area to cover because of interconnection wire present in between ICs.

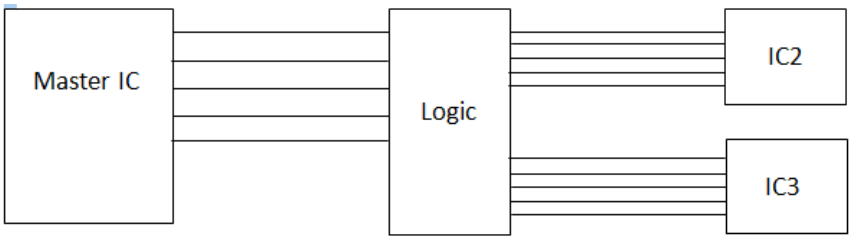

Fig 1.Basic block diagram of I^2C system

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These wire requirement can be reduce by using I²C,that is Inter-Integrated circuit bus. This communication have a special protocol assigned to it which is I ²C Protocol. I²C bus physically consist of two active wires and a ground connection. The two active wires namely Serial Clock[SCL] and Serial Data[SDA]. These wire are bidirectional half duplex in nature which carry information between the devices connected to the bus. Each device is acknowledge by a unique address whether it is a microcontroller, LCD driver, memory or keyboard interface and can operate as either a transmitter or receiver, depending on the function of t he device. In I²C bus devices can easily added or removed which is very useful for low maintenance and control application in embedded system

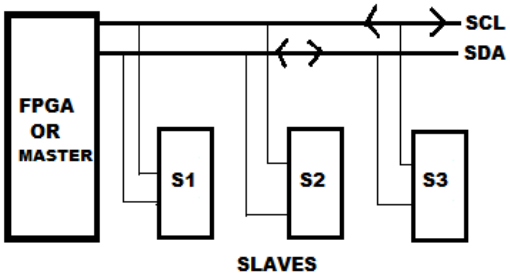

Fig 2.Master and Slave in I2C system

3. PROPOSED SYSTEM

Components Of I²C:

-I²C master top comprises of prescale register, command register, status register, transmit register, and receive register. Prescale register is used to reduce high frequency electrical signal to lower frequency by integer division. Data comes initially into status register and depending upon it the command register issues the commands. Transmit and receive register decide whether to transmit or receive the data and this data is transmitted parallel to data I/O register

-I²C Master Byte Controller are the byte command controller and data I/O shift register. The byte command controller is the heart of I²C communication traffic at the byte level and is a state machine that generates different states of I²C byte operations based on the command register bits. The data I/O shift register is a component which contains and deals with the data associated with the present I²C write and read transactions.

- I²C Master bit controller involves clock generator and a bit command controller. During transmission data is shifted bit by bit into the command bit controller and from there it is transferred onto SDA. During reception data comes on SDA and then to bit controller

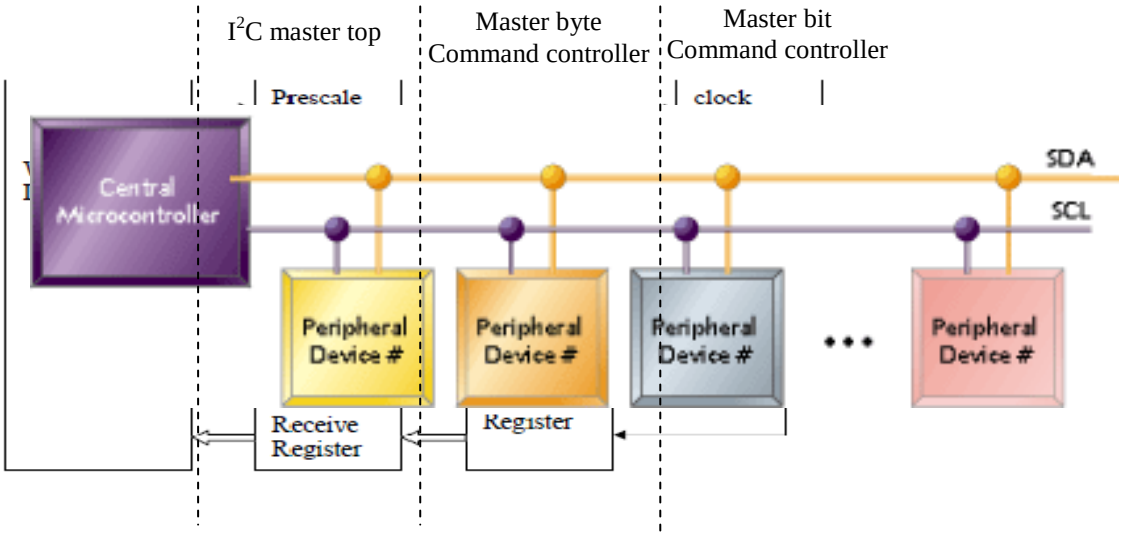

Fig 3: Components in I²C communication

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4. WORKING

Diffrent stages of I^2C communication are as explained below-

4.1. Start and Stop Conditions

Before any transaction a START condition needs to be issued on the bus. The start condition acts as a signal to all connected IC's that something is about to be transmitted.After a message has been completed, a STOP condition is sent. This is the signal for all devices on the bus that the bus is available again (idle). If a chip was accessed and has received data during the last transaction, it will now process this information (if not already processed during the reception of the message).

(a) Start	SDA SCL	The chip issuing the START condition first pulls the SDA line low and then pulls the SCL line low.	(b)Stop	SDA SCL	The bus master first releases the SCL line and then the SDA line in order to issue the STOP condition.

Table II: Start and Stop conditions

4.2. Transmitting a byte to a slave device

After start condition has been sent, a byte can be transmitted to a slave by the master. This first byte after a start condition will identify the slave on the bus (address) and will select the mode of operation. The meaning of all following bytes depends on the slave.

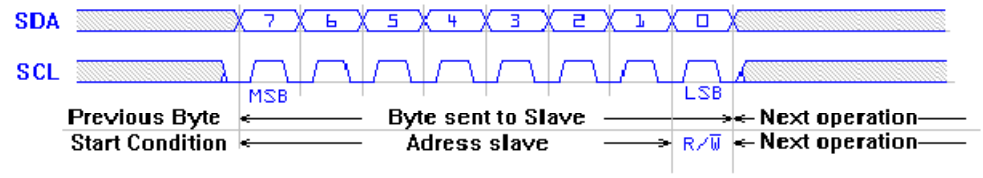

Fig 5: Transmission of a byte to a slave

4.3. Receiving a byte from a slave device

Once the slave has been addressed and the slave has acknowledged this, a byte can be received from the slave if the R/W bit in the address was set to READ (set to '1').

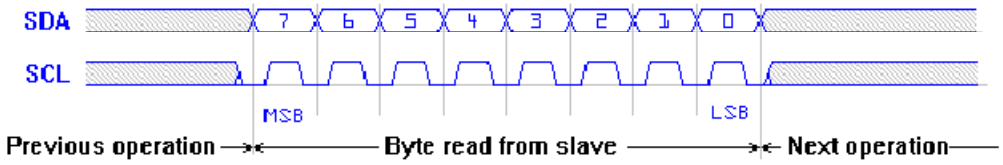

Fig 6: Reception of a byte from a slave

4.4 .Getting acknowledge (ACK) from a slave device

When an address or data byte has been transmitted onto the bus then this must be acknowledged by the slave(s). In case of an address, if the address matches its own then that slave and only that slave will respond to the address with an ACK. In case of a byte transmitted to an already addressed slave, the slave will respond with an ACK as well.

4.5. Giving acknowledge (ACK) from a slave device

Upon reception of a byte from a slave, the master must acknowledge this to the slave device. If there is no data left to receive, the master will send a not-acknowledge (NACK) signal and will stop the data transaction.[1]

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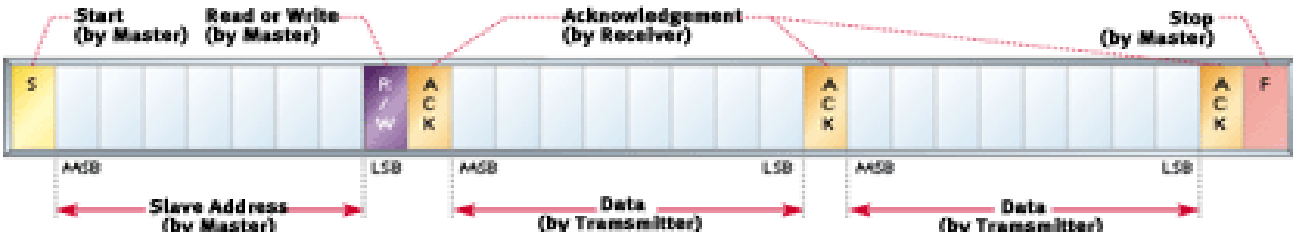
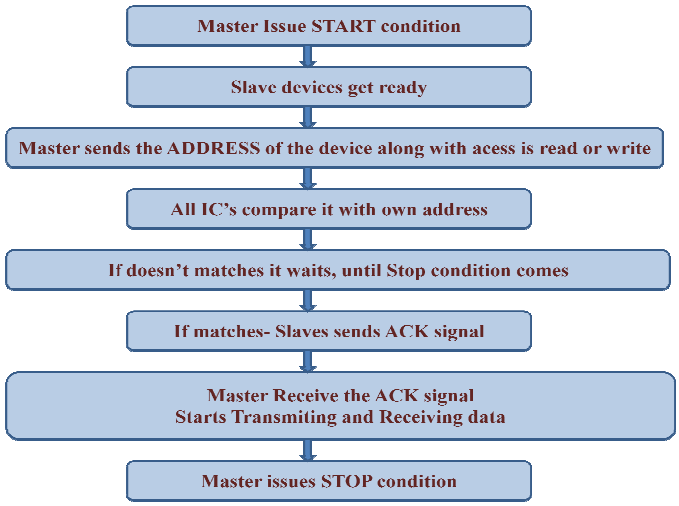


Fig7:Byte structure

4.6. Process Algorithm:



The overall coding part can be written on VHDL and simulate on Xilinx. It can be represented with the help of RTL diagram of I2C and verified. I2C interfacing technique is implemented using different techniques and Result can be verified with Xilinx ISE Design suite 13.1_1 .[1]

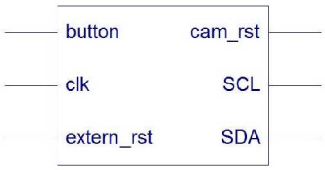


Fig 8: RTL diagram of Data Surveillanc

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S.No	Pin Name	Pin Description
1.	Button	It used for reset The FPGA
2.	Clk	It is the clock given for entire system
3.	Extern_rst	It is the external reset to restart the system
4.	CAM_RST	It is the camera reset signal to reset the camera
5.	SCL	It is the Serial Clock line to provide the clock
6.	SDA	Serial Data line, It send the address of the register

Table III: I/O Pin description

5. FEATURES OF I^2C

- It is multimaster serial ended computer bus
- I^2C has two wire bi-directional serial bus
- It is a simple and efficient method of data exchange
- I^2C protocol have low bandwith
- It is a Short distance protocol

6. ADVANTAGES OF I^2C

- Used for security sensitive applications like sensor connections, RFID, biometric devices, etc
- Common communication standards between microcontrollers and sensors
- Each device is recognised by its unique address and can operates as either a transmitter or receiver, depending upon the function of the device
- It Provides enhance security system
- Compatible with FPGA

7. CONCLUSION

The ideal surveillance architecture with I2C will have the following characteristics: high performance, flexibility, easy upgradability, low development cost, and a migration path to lower cost as the application matures and volume ramps. FPGAs in conjunction with the feature-rich Data and Image Processing Suite, Data over IP reference design, and partner's compression solutions offer data system designers all the key building blocks needed to produce such a system.

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